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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,553	06/20/2001	Lars-Peter Heineck	GR 98 P 1379 D	6319

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,553	HEINECK ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with Remarks filed 7/21/03 have been fully considered but they are not persuasive. In particular, the differences between Sun et al and the invention as pointed out by Applicants on pages 4-6 of said Remarks are not reflected in the claim language. The two aspects of the claim language that have received emphasis in said Remarks by underscoring are:

(a) "a gate....having at least one side wall adjacent at least one of said conductive regions"; and

(b) said gate oxide....having a thickened area in a region below said side wall of said gate" (see page 2 of said Remarks).

However, although no specific traverse has been formulated on the basis of the previous office action and the specific citations pertaining to the underscored aspects, it is herewith once more pointed out with reference to Figure 19 that:

Ad (a): the gate 6/18 (cf. column 5, lines 34-37 and column 7, lines 65-67) in Sun et al has at least one side wall (interface with 23; cf. column 8, lines 40-42 and Figure 19) adjacent at least one of said conductive regions 24 (i.e., the side wall of 6/18 by 23 is adjacent 24) (all of the specific references having been made in the previous office action): see Figure 19; and

Ad (b): the gate oxide 5/14 (cf. column 5, lines 24-33 and column 7, lines 12-27) in Sun et al has a thickened area in a region below said side wall of said gate (cf. Figure 19), i.e., below the interface between regions 6 and 23; all specific references having been made in the previous office action.

Consistent with the above considerations the rejections made in the previous office action are herewith repeated.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1 and 3-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al (5,612,249) in view of Joseph et al (5,907,777).

With regard to claim 1: Sun et al teach (cf. Figure 19 and column 8, lines 40-53) a MOS transistor that may be used as a single-transistor memory cell, comprising:

a semiconductor substrate 1 (cf. column 4, lines 50-52) having a substrate surface, a first conductive region and second conductive region (source and drain regions 24, see column 8, lines 48-52);

a gate oxide 5/14 (cf. column 5, lines 24-33 and column 7, lines 12-27; note that the material constitution of regions 5 and 14 are prescribed in identical manner: both regions are to be made by oxidation of silicon; hence from the device point of view the regions 5 and 14 constitute a contiguous entity) disposed on said substrate surface;

a gate 6/18 (cf. column 5, lines 34-37 and column 7, lines 65-67: note that regions 6 and 18 both materially are defined in exactly the same manner: they should consist of either poly or amorphous silicon; the distinction between gate 6 and interconnect 18 is thus from a device point of view moot, as both regions are materially identically specified and are, as gate and gate interconnect, required to have the same electrically conductive requirements) disposed on said gate oxide over an area between said first and second conductive regions (cf. Figure 19) and having at least one side wall (namely its interface with region 23), said sidewall being adjacent at least one of said conductive regions 24 (i.e., said sidewall between regions 5 and 23 is adjacent to region 24;

an oxide passivation layer 23 (cf. column 8, lines 40-42) disposed on said sidewall of said gate;

said gate oxide insulating said gate (note that the material constitution of the gate oxide is prescribed as the product of the oxidation of silicon, hence silicon oxide; see column 5, line 27; and column 7, lines 12-15) and having a thickened area below said sidewall 23 of said gate.

Sun et al do not necessarily teach the further limitations that (a) specifically said oxide passivation layer is a silicon dioxide passivation layer, and that (b) an insulating

silicon nitride spacer be disposed on said oxide passivation layer, said (insulating silicon nitride) spacer acting as oxidation barrier.

However, ad (a): Sun et al do advocate thermal oxidation of silicon to be a viable method to produce thin SiO_2 films that can be used in conjunction with thermal nitridation of silicon (silicon nitride films) to create easily controllable, effective barriers (cf. column 2, lines 2-9); the selection of *silicon* oxide is thus an obvious one within the context of the patent to Sun et al; *furthermore, ad (b)*: as shown by Joseph et al (cf. Figure 7, column 4, lines 15-22 and column 5, lines 8-19), it has long been known in the art of insulated gate field effect transistors that it is advantageous to apply an additional silicon nitride layer (cf. column 4, line 16) over a silicon (di)oxide passivation layer 302 (cf. column 5, line 29) protecting the sidewall of an insulated gate, for the specific purpose of preventing the migration or diffusion of ions (cf. column 5, lines 15-16).

Motivation to include the teaching in this regard by Joseph et al is the prevention of the deterioration of the insulating quality of the gate oxide; *combination* of said teaching with the invention by Sun et al is straightforward, as it only requires the retention of an intermediate structure, as exemplified by Figure 15 in Sun et al (particularly, layers 11 and 13). *Success* in implementing said teaching can thus be reasonably expected.

Finally, the (insulating silicon nitride) spacer inherently acts like an oxidation barrier to the same extent as it does in Applicant's specification, given the same topographic conditions in its surroundings, while the structure defines how it can act,

and hence the structure is not additionally defined by line 14 of claim 1 ("...acting as an oxidation barrier").

With regard to claim 3: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67). Therefore, the further limitation as defined in claim 3 does not distinguish over the prior art.

With regard to claim 4: Sun et al teach a layer of tungsten-silicide film 20 deposited on the polysilicon gate layer 18 (see Figure 17 and column 8, lines 13-18). Therefore, the primary reference teaches the further limitations defined by claim 4.

With regard to claim 5: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67).

With regard to claim 6: said gate taught by Sun et al is specifically allowed to include a tungsten silicide layer (column 8, lines 13-18 and Figure 17) and a polysilicon layer (cf. column 5, lines 34-37 and column 7, lines 65-67).

2. ***Claims 7-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al and Joseph as applied to claims 6 and 1, respectively above, and further in view of Krautschneider ((5,854,500). As detailed above, claims 1 and 6 are unpatentable over Sun et al, in view of Joseph et al. Sun et al nor Joseph et al necessarily teach the further limitation of claims 7 or 8. As shown by Krautschneider (front figure), however, lateral MOS transistors with attributes as essentially taught by the combination of the inventions of Sun et al and Joseph et al, particularly with gate oxide 110 (see in

Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20), for instance, have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of said combinations of inventions.

Conclusion

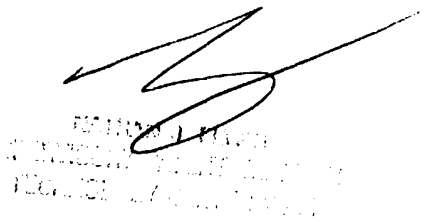
2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



JPM
October 8, 2003